REMARKS

Claims 1-9 and 11- 20 are in the application. Claim 10 is cancelled by this amendment. Claims 16-20 have been withdrawn in view of a restriction requirement.

By this amendment, specification has been amended to fix several minor typographical errors. Also, the title has been amended in view of the restriction requirement. Additionally, claims 1, 2, 4-9, and 11-15 have been amended either to more particularly claim the subject matter in which applicants believe their invention pertains to, or to fix minor typographical errors.

Response to First 35 U.S.C. §103 Rejection

Claims 1-4, 6-13, and 15 were rejected under 35 U.S.C. §103 as being unpatentable over Wang et al., USP 6,365,924 (hereinafter "Wang") in view of Mori, USP 4,246,594 (hereinafter "Mori"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 has been amended to call for a high frequency integrated circuit structure comprising a body of semiconductor material having a plurality of isolated active regions. The body semiconductor material has a first conductivity type. Internal circuitry is formed in a first active region. A second active region comprising a buried layer of a second conductivity type is formed over the body of semiconductor material and a first semiconductor layer of the second conductivity type is formed over the buried layer. The first semiconductor layer has a lower dopant concentration than the buried layer.

A first silicon controlled rectifier device is formed in the second active region. The first silicon controlled rectifier device comprises a first well region of the first conductivity type formed in the first semiconductor layer, a first doped region of the first conductivity type formed in the first well region, the buried layer, a second well region of the first conductivity type formed in the first semiconductor layer and spaced apart from the first well region, and a second doped region of the second conductivity type formed in the second well region.

A second silicon controlled rectifier device comprises the second well region, a third doped region of the first conductivity type formed in the second well region, the buried layer, the first well region, and a fourth doped region of the second conductivity type formed in the first well region.

The first and second silicon controlled rectifier devices are coupled to the internal circuitry and form an ESD structure for protecting the internal circuitry against positive and negative ESD stresses.

Applicants respectfully submit that Wang in view of Mori fails to make claim 1 obvious for several reasons. First, Wang as the primary reference fails to show or suggest, among other things, a buried layer of a second conductivity type and a first semiconductor layer of the second conductivity type formed over the buried layer, wherein the first semiconductor layer has a lower dopant concentration than the buried layer. Wang is silent on this limitation. Specifically, Wang teaches a conventional diffused n-well 116, which has a conventional diffused dopant profile.

Applicants further submit that this is not a minor difference because with their implementation, the buried layer provides, among other things, a relatively high holding voltage, which allows applicants' structure to overcome deficiencies of prior art structure like Wang's, which have a tendency to remain in a clamped "on" state when parasitic triggering events occur (see paragraphs **[0027]** and **[0040]** in applicants' specification).

Moreover, applicants assert that there is no motivation to combine the two references because the Wang reference teaches a CMOS implementation (see column 4, line 31) of a dual direction SCR device, while Mori teaches a conventional unidirectional bipolar SCR switch. Additionally, Mori's SCR structure is not symmetrical and thus is not conducive to forming an ESD structure for protecting internal circuitry against positive and negative ESD stresses. Specifically, Mori's structure has an individual SCR in each cell, and these individual SCR's comprise lateral PNPN devices (regions 14, 18, 20, and 22), which are not symmetrical as evident in FIG. 3a.

Thus, for at least these reasons, applicants respectfully submit that claim 1 is allowable.

Claims 2-3 depends from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 4 depends from claim 2 and further calls for a deep contact trench extending from a surface of the first semiconductor layer into the semiconductor wafer. Claim 4 is believed allowable for the same reasons as claim 1. Additionally, applicants respectfully submit that claim 4 is allowable because neither Wang nor Mori teach or suggest a deep contact trench extending from a surface of the first semiconductor layer into the semiconductor wafer.

Claims 6 and 7 depend from claims 1 and 2 and are believed allowable for at least the same reasons as claims 1 and 2.

Claim 8 depends from claim 1 and further calls for a deep isolation trench formed in the body of semiconductor material for isolating the ESD structure from the internal circuitry, wherein the isolation trench includes a dielectric layer. Claim 8 is believed allowable for the same reasons as claim 1. Additionally, applicants respectfully submit that claim 8 is allowable over Wang and Mori because neither reference shows or suggests a deep isolation trench that includes a dielectric layer.

Claim 9 has been amended and now calls for a symmetrical SCR device comprising a semiconductor substrate of a first conductivity type. A first semiconductor layer of the first conductivity type is formed over the semiconductor substrate, wherein the first semiconductor layer has a lower dopant concentration than the semiconductor substrate. A second semiconductor layer of a second conductivity type is formed adjacent the first semiconductor layer. A third semiconductor layer of the second conductivity type is formed adjacent the second semiconductor layer, wherein the third semiconductor layer has a lower dopant concentration than the second semiconductor layer.

First and second wells comprising a second conductivity type are formed in the third semiconductor layer, wherein the first and second wells are spaced apart. First and second doped regions are formed in the first well, wherein the first doped region comprises the first conductivity type and the second doped region comprises the second conductivity type, and wherein the first and second doped

regions are coupled. Third and fourth doped regions are formed in the second well, wherein the third doped region comprises the first conductivity type and the fourth doped region comprises the second conductivity type, and wherein the third and fourth doped regions are coupled.

Applicants respectfully submit that Wang in view of Mori fails to make claim 9 obvious for several reasons. First, Wang as the primary reference fails to show or suggest, among other things, a second semiconductor layer of a second conductivity type and a third semiconductor layer of the second conductivity type formed over the second semiconductor layer, wherein the third semiconductor layer has a lower dopant concentration than the second semiconductor layer. Wang is silent on this limitation. Specifically, Wang teaches a conventional diffused n-well 116, which has a conventional diffused dopant profile.

Applicants further submit that this is not a minor difference because with their implementation, the second semiconductor layer provides, among other things, a relatively high holding voltage, which allows applicants' structure to overcome deficiencies of prior art structures like Wang's, which have a tendency to remain in a clamped "on" state when parasitic triggering events occur (see paragraphs **[0027]** and **[0040]** in applicants' specification).

Moreover, applicants assert that there is no motivation to combine the two references because the Wang reference teaches a CMOS implementation (see column 4, line 31) of a dual direction SCR device, while Mori teaches a conventional unidirectional bipolar SCR switch. Additionally, Mori's SCR structure is not symmetrical as is called for in claim 9. Specifically, Mori's structure has an individual SCR in each cell, and these individual SCR's comprise unidirectional

lateral PNPN devices (regions 14, 18, 20, and 22), which are not symmetrical as evident in FIG. 3a.

Thus, for at least these reasons, applicants respectfully submit that claim 9 is allowable.

Claim 10 has been cancelled by this amendment.

Claims 11 and 12 depend from claim 9 and are believed allowable for at least the same reasons as claim 9.

Claim 13 depends from claim 9 and further calls for a deep contact trench extending from a surface of the third semiconductor layer into the semiconductor substrate. Claim 13 is believed allowable for the same reasons as claim 9. Additionally, applicants respectfully submit that claim 13 is allowable over Wang and Mori because neither reference teaches or suggests a deep contact trench extending from a surface of the third semiconductor layer into the semiconductor substrate.

Claim 15 depends from claim 9 and is believed allowable for at least the same reasons as claim 9.

Response to the Second 35 U.S.C. §103 Rejection

Claims 5 and 14 were rejected under 35 U.S.C. §103 as being unpatentable over Wang in view of Mori as applied to claims 1, 2, and 9 above, and further in view of Duvvury et al., USP 6,365,940 (hereinafter "Duvvury"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 5 depends from claim 1 and is believed allowable for at least the same reasons as claim 1. Specifically, Duvvury does not make up for the deficiencies of Wang as set forth above.

Claim 14 depends from claim 9 and is believed allowable for at least the same reasons as claim 9. Specifically, Duvvury does not make up for the deficiencies of Wang as set forth above.

In view of all of the above, it is believed that the claims are allowable, and the case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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